CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the subject application.

AMENDMENTS TO THE CLAIMS:

1. **(Currently Amended)** A method in an emulation system, comprising:

receiving a first sample of state data, the first sample of state data having a plurality of bits and being descriptive of one or more states in an emulation system;

~~selecting~~ identifying a first data of interest ~~from~~ in the first sample of state data, wherein the first data of interest is a ~~first~~ subset of the plurality of bits of the first sample of state data ~~and includes at least first and second portions separated from each other by at least one bit that is not part of the first data of interest~~;

identifying first ignored data in the first sample of state data, the first ignored data being a subset of the bits of the first sample of state data and different from the first data of interest;

determining if residual storage space in a first buffer exists; and

~~storing the first data of interest from the first sample of state data in said first buffer~~ if it is determined that residual storage space in the first buffer exists, sorting the first data of interest from the first ignored data by storing the first data of interest in the first buffer, and

if it is determined that residual storage space in the first buffer does not exist, sorting the first data of interest from the first ignored data by storing the first data of interest in a second buffer~~such that the first and second portions of the first data of interest as stored are no longer separated from each other by the at least one bit, and otherwise storing said first data of interest in a second buffer such that the first and second portions of the data of interest as stored are no longer separated from each other by the at least one bit~~;

~~receiving a second sample of state data; and~~

~~selecting a second data of interest from the second sample of state data, wherein the second data of interest is a second subset of bits of the second sample of state data and wherein bit locations of the first data of interest and the second data of interest are different.~~

2. **(Currently Amended)** The method of claim 1, further comprising:

receiving a second sample of state data;

identifying second data of interest in the second sample of state data, the second data of interest being a subset of the plurality of bits of the second sample of state data;

determining if residual storage space in ~~whether~~ the first buffer exists ~~is full~~ after storing the first data of interest in the first buffer ~~from the first sample in the first buffer.~~; and

if it is determined that residual storage space in the first buffer exists, storing at least a portion of the second data of interest in the first buffer after storing the first data of interest in the first buffer, and

if it is determined that residual storage space in the first buffer does not exist, storing at least a portion of the second data of interest in the second buffer.

3-7. **(Previously Canceled)**

8 - 10. **(Canceled)**

11-15. **(Previously Canceled)**

16. **(Currently Amended)** The method of claim 1, further comprising:

identifying information associated with the first data of interest; and

storing the information ~~associated with the first sample of state data~~ to a memory storage location.

17. **(Currently Amended)** The method of claim 16, wherein the information comprises a bit position of the first data of interest within ~~of~~ the first sample of state data.

18. **(Previously Presented)** The method of claim 16, wherein the information comprises an identification of a pin associated with the first sample of state data.

19. **(Currently Amended)** The method of claim 16,

the second data of interest includes at least first and second portions separated from each other within the second sample of state data by at least one bit that is not part of the second data of interest;

the first and second portions of the second data of interest being stored such that they are no longer separated from each other by the at least one bit; and wherein:

the method further comprises ~~comprising~~ identifying information associated with the second data of interest and storing the information to a memory storage location.

~~selecting the second data of interest from the second sample of state data, wherein the second data of interest and includes at least third and fourth portions separated from each other by at least one bit that is not part of the second data of interest~~

~~storing the second data of interest from the second sample of state data;~~

~~storing information associated with the first sample of state data in memory; and~~

~~storing information associated with the second sample of state data in memory.~~

20. **(Currently Amended)** An apparatus, comprising:

a first select logic device configured to receive samples of state data, to ~~select~~ identify data of interest from each of the samples of state data, the data of interest having non-contiguous bits, and further configured to sort the data of interest such that the non-contiguous bits become contiguous, ~~wherein selected bit locations of the data of interest from at least two samples are different~~, wherein

the sorting results in a contiguous set of bits of interest and a contiguous set of ignored bits, the contiguous set of bits of interest being different from the contiguous set of ignored bits;

first and second buffers coupled to the first select logic device and configured to receive the contiguous set of bits of interest ~~sorted data of interest in an alternating manner~~ by filling the first and second buffers in an alternating manner, wherein the filling results in the contiguous set of ignored bits not being preserved by the first select logic device;

a second select logic device coupled to the first and second buffers and configured to select the first and second buffers in an alternating manner to drain the selected buffer; and

an output storage device coupled to the second select logic device and configured to receive data drained from the selected one of the first and second buffers.

21. **(Original)** The apparatus of claim 20 wherein the first select logic comprises a multiplexer.

22. **(Original)** The apparatus of claim 20, wherein the second select logic device comprises a multiplexer.

23. **(Original)** The apparatus of claim 20, wherein the first select logic device is configured to send the contiguous set of bits ~~data of~~ interest to the second buffer responsive to the first buffer becoming full.

24. **(Original)** The apparatus of claim 20, wherein the first select logic device comprises a data of interest sorter.

25. **(Previously Presented)** The apparatus of claim 20, further comprising: a memory configured to store information associated with the samples of state data.

26. **(Currently Amended)** The apparatus of claim 25, wherein the information comprises at least a bit position of data of interest ~~of~~ within the samples of state data.

27. **(Previously Presented)** The apparatus of claim 25, wherein the information comprises an identification of a pin associated with each of the samples of state data.

28. **(Previously Presented)** The apparatus of claim 20, wherein the output storage device is configured to store information associated with each of the samples of state data.

29. **(Currently Amended)** A method for associating trace data chains with pins of an integrated circuit, the method comprising~~: steps of:~~

determining a trace data fill rate of each of a plurality of trace data chains; and

determining a schedule for associating a plurality of pins with the plurality of trace data chains to transfer data out of the trace data chains based at least upon the determined trace data chain fill rates, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins change from a first clock cycle to a second clock cycle.

30. **(Currently Amended)** In an emulation debugging resource, a method comprising:

determining fill rates of a plurality of trace data chains;

determining a schedule for associating a plurality of pins with the plurality of trace data chains based at least upon the determined fill rates; and

associating a set of the plurality of trace data chains with the plurality of pins in accordance with the determined schedule, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins change from a first clock cycle to a second clock cycle.

31. **(Currently Amended)** In an integrated circuit, the integrated circuit including an emulator, an apparatus comprising:

a plurality of trace data chains;

a trace pin select logic device coupled to the plurality of trace data chains to select a set of the plurality of trace data chains;

a plurality of pins; and

a memory coupled to the trace pin select logic device and configured to store a schedule to associate the selected set with the pins based at least upon determined trace data chain fill rates of the set, wherein one of the plurality of pins is shared by at least two trace data chains and wherein the plurality of pins change from a first clock cycle to a second clock cycle.

32. **(Canceled)**